

**AMENDMENTS TO THE CLAIMS:**

**Complete Listing of Claims**

1      Claim 1. (previously presented) A microcontroller integrated circuit (IC)  
2      comprising:  
3                a program memory for storing a program to be executed;  
4                a program counter coupled to the program memory for selecting address  
5      locations in said memory;  
6                a program counter copy register for storing a program memory address  
7      pointed to by said program counter as a return address from a debug monitor  
8      routine;  
9                instruction execution circuitry coupled to the program memory for  
10     executing instructions received from said memory;  
11               a breakpoint address register for storing a breakpoint address;  
12               address compare circuitry for comparing a value in said program counter  
13      to a value in said breakpoint address register, said compare circuitry providing a  
14      breakpoint signal upon detection of a valid breakpoint address comparison; and  
15               a multiplexer interposed between said program memory and said program  
16      execution circuitry, said multiplexer comprising circuitry for inserting a debug  
17      instruction into the instruction execution circuitry upon receipt of said breakpoint  
18      signal, wherein said debug instruction is substituted for an instruction in a  
19      program memory address pointed to by said program counter.

1      Claim 2. (original)   The microcontroller IC of claim 1, further comprising:  
2            a stack pointer register;  
3            a stack breakpoint register for storing a stack trap address;  
4            stack pointer compare circuitry for comparing a value in said stack pointer  
5        register to a value in said stack breakpoint register, said stack pointer compare  
6        circuitry providing a stack trap signal upon detection of a valid stack pointer  
7        address comparison; and  
8            wherein said multiplexer inserts said debug instruction into the instruction  
9        execution circuitry upon receipt of said stack trap signal.

1      Claim 3. (original)   The microcontroller IC of claim 2, wherein said valid stack  
2        pointer address comparison is selected from the group consisting of: said value  
3        in said stack pointer register being equal to said value in said stack breakpoint  
4        register, said value in said stack pointer register being greater than said value in  
5        said stack breakpoint register, said value in said stack pointer register being less  
6        than said value in said stack breakpoint register, and combinations thereof.

1      Claim 4. (original)   The microcontroller IC of claim 1, further comprising single  
2        step circuitry directing said multiplexer circuitry to insert said debug instruction  
3        into the instruction execution circuitry after the execution of each instruction of an  
4        application program.

1      Claim 5. (original)   The microcontroller IC of claim 1, wherein said debug  
2        instruction is a long jump instruction to a debug monitor routine.

Claim 6 (canceled)

1      Claim 7. (original)   The microcontroller IC of claim 1, wherein said address  
2      comparison circuitry further comprises memory bank comparison circuitry for  
3      detecting a specific bank access in addition to said breakpoint address.

1      Claim 8. (previously presented)   An embedded microcontroller apparatus  
2      comprising:  
3                a circuit board embedded in the apparatus;  
4                a microcontroller integrated circuit disposed on said circuit board,  
5      including  
6                a program memory for storing a program to be executed,  
7                a program counter coupled to the program memory for selecting address  
8      locations in said memory,  
9                a program counter copy register for storing a program memory address  
10     pointed to by said program counter as a return address from a debug monitor  
11     routine, and  
12                debug circuitry disposed on said microcontroller integrated circuit, said  
13     debug circuitry comprising  
14                compare circuitry for comparing a breakpoint address to instruction  
15     fetch addresses in said program memory, said compare circuitry  
16     generating a breakpoint signal indicating a valid address compare; and  
17                multiplexer circuitry coupled to said compare circuitry, said  
18     multiplexer circuitry, upon receiving said breakpoint signal, substituting a  
19     debug program instruction for execution by the microcontroller in place of  
20     a standard instruction fetched from program memory.

1      Claim 9. (original)   The embedded microcontroller apparatus of claim 8,  
2      wherein said apparatus is a universal serial bus controller.

1      Claim 10. (original) The embedded microcontroller apparatus of claim 8,  
2      wherein said microcontroller further comprises a stack pointer register, and said  
3      debug circuitry further comprises:

4                a stack breakpoint register for storing a stack trap address; and  
5                stack pointer compare circuitry for comparing a value in said stack pointer  
6      register to a value in said stack breakpoint register, said stack pointer compare  
7      circuitry providing a stack trap signal upon detection of a valid stack pointer  
8      address comparison; wherein said multiplexer substitutes said debug program  
9      instruction for execution by said microcontroller upon receiving said stack trap  
10     signal.

1      Claim 11. (original) The embedded microcontroller apparatus of claim 10,  
2      wherein said valid stack pointer address comparison is selected from the group  
3      consisting of: said value in said stack pointer register being equal to said value in  
4      said stack breakpoint register, said value in said stack pointer register being  
5      greater than said value in said stack breakpoint register, said value in said stack  
6      pointer register being less than said value in said stack breakpoint register, and  
7      combinations thereof.

1      Claim 12. (original) The embedded microcontroller apparatus of claim 8, said  
2      debug circuitry further comprising single step circuitry directing said multiplexer  
3      circuitry to substitute said debug program instruction for execution by said  
4      microcontroller after the execution of each standard instruction fetched from  
5      program memory.

1      Claim 13. (original) The embedded microcontroller apparatus of claim 8,  
2      wherein said debug program instruction is a long jump instruction to a debug  
3      monitor routine.

Claim 14 (canceled)

1     Claim 15. (previously presented) A method of debugging a microcontroller  
2     integrated circuit, said method comprising:  
3                 storing a breakpoint address in a hardware register on said microcontroller  
4     integrated circuit;  
5                 executing an application program from program memory by said  
6     microcontroller;  
7                 comparing application program instruction addresses to said breakpoint  
8     address;  
9                 halting execution of said application program upon detection of an  
10   instruction fetch from a memory address equal to said breakpoint address;  
11                 storing said memory address in a program counter copy register, wherein  
12   said address is reloaded into said program counter after execution of said debug  
13   routine;  
14                 substituting a jump instruction to a debug program for said instruction  
15   fetched from said memory address; and  
16                 executing said debug program.

1     Claim 16. (original) The method of claim 15, further comprising:  
2                 storing a stack trap address in a stack breakpoint hardware register on  
3     said microcontroller;  
4                 comparing stack pointer addresses to said stack breakpoint address; and  
5                 upon detection of a valid stack pointer address comparison, performing  
6   said halting execution, said substituting said jump instruction, and said executing  
7   said debug program steps.

1    Claim 17. (original) The method of claim 16, wherein said valid stack pointer  
2    address comparison is selected from the group consisting of: said stack pointer  
3    address being equal to said stack breakpoint address, said stack pointer address  
4    being greater than said stack breakpoint address, said stack pointer address  
5    being less than said stack breakpoint address, and combinations thereof.

1    Claim 18. (original) The method of claim 15, said executing said debug program  
2    comprising:  
3         providing status information to external circuitry; and  
4         receiving new breakpoint address information.

Claim 19 (canceled)

1    Claim 20. (previously presented) The method of claim 15, further comprising  
2    pushing the address stored in the program counter copy register onto a stack  
3    and executing a return to said application program at a location pointed to by  
4    said memory address.